REMARKS

Claims 1-18 are pending. Claims 6-11 have been withdrawn from consideration. Reconsideration and allowance in view of the following remarks are respectfully requested.

Specification

The Office Action objects to claims 6-9 because the status was incorrectly identified. Applicants have noted that claims 6-9 have the status of "withdrawn" and have identified them as such. Accordingly, withdrawal of the objection is respectfully requested.

Prior Art Rejection

The Office rejects claims 1, 13, 14, 16 and 17 under 35 U.S.C. §103(a) as being unpatentable over Kuroda (US 5,487,029) in view of Clemons, (US 4,599,709); claims 2-5 under 35 U.S.C. §103(a) as being unpatentable over Clemons, Kuroda and Dierke; and claims 12, 15 and 18 under 35 U.S.C. §103(a) as being unpatentable over Kuroda, Clemons and Seyyedy (US 5,969,380). These rejections are respectfully traversed.

For reasons of brevity applicants' previous remarks filed on December 27, 2006 are hereby incorporated by reference.

Claims 1, 12 and 13 recite, *inter alia,* each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective

different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment.

Kuroda teaches bit lines being segmented such that within each block, a group of eight memory cells connected to one bit line is switched by switching transistors Q1, for instance as depicted in fig. 1 to a connection with a through-going data line for input/output and running through the two blocks of a column. When a read operation is performed, e.g. a block 01 (with reference to fig. 1 of Kuroda), i.e. the first block in row 1 is selected by pulsing a selector word line WB 1 high and making any of the switches Q1, Q2 etc. conducting and thus establishing an ohmic contact with designated bit lines joining the data lines DO, Dl,...D7 via respectively switching transistors Q1, Q2...Q3 as depicted. Simultaneously the Y decoder pulls selector line Y0 high, allowing transistor Q4 to conduct such that the data line and consequently a bit line in block 01 can be placed at appropriate potential. The transistor Q5 at the same time also becomes conducting connecting the data line DO in this case with a sense amplifier SA in the control block (actually WRCO block) at the bottom of the column. By now setting e.g. the word line W10 to an appropriate potential the memory cell connected between this word line and the bit line adjoined to the switching transistor Q1 and the data line D0 shall allow a sensing of the logical value or datum stored as a charge in the ferroelectric capacitor constituting the memory cell. Consequently a charge response corresponding to the logical value stored is output to the sense amplifier SA.

At most in Kuroda's system eight (8) memory cells of a bit line segment within a block can be in an established electrical circuit between word lines and the data line. This is the case when the eight

memory cells on the bit line are switched by transistor Q1 to contact with the data line D0 in fig. 1. The object of Kuroda's invention is to reduce the number of switching transistors to a minimum, but at the same time being able to maintain as low level of voltage disturb as possible. Thus, as shown in fig. 1 of Kuroda at most 8 memory cells of each block in a row at a time can be fully connected in the RC network. It should be noted that a passive matrix-addressable ferroelectric memory is eminently suitable for parallel addressing operations as all memory cells on a world line can be addressed for read or write simultaneously. This is, however, not the case for Kuroda. Only one sense amplifier SA is connectable with a column and this means that only one memory cell in one column can be read at a time and consequently also thus at most 8 cells of the separate eight blocks of a row can be read simultaneously. This would entail that 64 memory cells simultaneously are switched into contact with the RC network, but only 8 of these are selected for an addressing operation, and the remainder 56 non-selected cells shall thus be prone to voltage disturb.

Clemons, in contrast with Kuroda does not disclose a ferroelectric memory, but rather a static random access memory allowing a multiple bit organization. Applying the bytewise addressing organization of Clemons & al. to the architecture of Kuroda, which discloses a rather different type of memory, namely what perhaps best could be termed a semi-active matrix-addressable ferroelectric memory, would entail a completely different organization of Kuroda's device and largely negate the advantages claimed by the latter. As amply evident from fig. 2 the static random access memory of Clemons of course is a wholly active matrix-addressable memory, as conventional with SRAMS.

The Examiner states that it would have been obvious at the time the invention was made to modify the device of Kuroda by incorporating the means of Clemons, connecting each bit lines assigned to a segment with an associated sensing means. However, it is rather the bit lines of Kuroda that are segmented so the modification would entail a complete redesigning of the data line selector block (i.e. equipped with transistors Q4....Q9 as depicted in fig. 1 of Kuroda) and the detecting driver block comprising the read and write amplifiers SA;WA as shown.

Applicants submit that one of ordinary skill would not look to teachings of Clemons and combine them with Kuroda to achieve a word line segmentation to achieve simultaneous read out of all corresponding word lines. As noted above Kuroda relies upon segmentation of eight memory cells (blocks), where this is a bit line, where each bit line corresponds to a single transistor gate for read out. In Clemons, each bite block is separated based on the bit lines. Each bit line is accessed using one of transistors T200 through T203 as illustrated for bite block one. The addressing of the voltage on the bit lines to specific sense amplifiers is not based on segmentation of the word lines. This is further noticed in Fig. 3 in which each segmented bit lines, referred to as bite block one through eight, is provided and connected to the IO switches. The number of word lines is inconsequential to both Kuroda and Clemons bit line segmentation. If Clemons was segmented based on the word lines then all eight crossings of the bit lines with the word lines corresponding to bite blocks 1-8 would be simultaneously sensed for each word line in the word line segmentation.

In applicant's invention, the word lines are segmented because of the unique nature posed by the passive matrix memories as discussed above. By segmenting the word lines, which allows for selection of all bit

lines associated with those word lines across each segment, each bit line is then associated with a specific sensing amplifier and read out.

Thus, applicants respectfully submit that the problem remains with the combination of Kuroda and Clemons not teaching or suggesting word line segmentation as claimed. Therefore, the combination of Kuroda and Clemons fails to teach or suggest each and every feature of claims 1, 12 and 13 as required.

Further, Dierke and Seyyedy fail to remedy the deficiencies of Kuroda and Clemons. Accordingly, applicants respectfully submit that neither Kuroda, Clemons, Dierke or Seyyedy alone or in combination teach or suggest the above claimed limitations. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

CONCLUSION

In view of the above amendment, applicants believe the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Chad J. Billings Reg. No. 48,917 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees

required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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